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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,011	11/26/2003	Christoph Heer	INF 2002 P 10624 US	7561
48154 7590 10/09/2007 SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			EXAMINER COUGHLAN, PETER D	
			ART UNIT 2129	PAPER NUMBER
			MAIL DATE 10/09/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10724011	11/26/2003	HEER, CHRISTOPH	INF 2002 P 10624 US

**EXAMINER**

Peter Coughlan

**ART UNIT****PAPER**

2129

09252007

DATE MAILED:


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**Commissioner for Patents**

The change from configurable logic blocks to circuits within the claims of this application bring to the surface numerous problems of the invention and its only diagram.

The Examiner called Mr. Matsil (Reg. No. 35272) on 9/21/2007 to have a Examiner initiated interview concerning the diagram and the lack of description within the specification of these circuits and how they work to achieve a 'if-then-else' statement.

Mr. Matsil never returned the Examiner's message.

  
**JOSEPH P HIRL**  
**PRIMARY EXAMINER**  
**TECHNOLOGY CENTER 2100**